IN THE CLAIMS:

Please amend Claims 1, 7, 9 and 18-20 as follows:

1. (AMENDED) A method of reducing circuit timing delays, comprising:

selecting a first node;

A1 sorting fanins of the first node according to slack values associated with the corresponding fanins, wherein at least a portion of the slack values differ in value; and

reducing delays associated with fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values.

7. (AMENDED) The method defined in Claim 6, wherein recursively reducing A2 delays is performed on critical fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values.

9. (AMENDED) A method of performing circuit delay reduction, comprising:

A3 performing a timing analysis on a circuit;

determining a delay target based at least in part on the timing analysis;

selecting a first output having a negative slack based at least in part on the delay target; and

performing local transformations on transitive fanins of the first output to improve the negative slack.

18. (AMENDED) The method defined in Claim 12, wherein the first PI node and the second PI node are the same.

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19. (AMENDED) The method defined in Claim 12, wherein the first PO node and the second PO node are the same.

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20. (AMENDED) The method defined in Claim 12, wherein a portion of the first critical path overlays a portion of the second critical path.

Please add the following new claims:

21. (NEW) A method of dynamically reducing delays on a critical path of a circuit topology, the method comprising:

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identifying a critical path of the circuit topology;

selecting a delay target for a primary output associated with the critical path;

reducing a first critical path delay beginning at a first node in closer proximity to a primary input associated with the critical path than to the primary output;

storing the reduced delay; and

reducing a second critical path delay beginning at a second node located between the first node and the primary output based at least in part on the stored reduced delay.

22. (NEW) The method defined in Claim 21, wherein the circuit topology is associated with a standard cell design process.

23. (NEW) The method defined in Claim 21, wherein the circuit topology is associated with a gate array design process.

24. (NEW) The method defined in Claim 21, wherein the circuit topology is associated with a programmable logic design process.

25. (NEW) A layout-driven logic synthesis design flow, comprising:

selecting a desired circuit delay associated with a first output of a circuit path;

calculating an initial circuit delay associated with the first output; and

iteratively reducing the initial circuit delay to achieve the desired circuit delay using a timing optimization process, wherein in an iteration, mapping and clustering are

used to measure the outcome of the timing optimization procedure, and wherein the timing optimization process uses such measurements to achieve the desired delay.

26. (NEW) The method defined in Claim 25, wherein the design flow is associated with a standard cell design process.

27. (NEW) The method defined in Claim 25, wherein the design flow is associated with a gate array design process.

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28. (NEW) The method defined in Claim 25, wherein the design flow is associated with a programmable logic design process.

29. (NEW) A method of performing a local transformation on a node in a circuit topology having at least one fanin cone and a critical fanin cone, the method comprising:

identifying a delay target for the node;

collapsing the critical fanin cone for the node based on a predetermined collapse depth;

determining if the delay target for the node is met; and

collapsing a fanin cone for the node based on the predetermined collapse depth if the delay target for the node is not met.

30. (NEW) The method defined in Claim 29, additionally comprising:

setting the collapse depth initially to a value of two; and

changing the collapse depth to a value of three if the delay target is not met.

31. (NEW) The method defined in Claim 29, additionally comprising performing timing-driven decomposition on the node prior to determining if the delay target is met.